Jianlei Yang

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Research Interests

- Computer-Aided Design (CAD) techniques for Integrated Circuits
- Numerical algorithms for circuit simulation, large scale power grid analysis and verification

Education

Sept. 2009 - July 2014	**Tsinghua University**, Beijing, China Ph.D Degree in Computer Science and Technology Electronic Design Automation Laboratory Advisor: Prof. **Yici Cai**
Sept. 2005 - July 2009	**Xidian University**, Xi'an, China Bachelor Degree in Microelectronics

Professional Experiences

July 2013 - July 2014	**Intel Labs China**, Beijing, China Intern: Embeded Architecture Group Project: IP power modeling, dynamic time warping (DTW)
July 2012 - August 2012	**Nimbus Automation Technologies**, Shanghai, China Intern: Develop DRC open checker and tie-pin router

Selected Research Contributions

1. *Early Stage Simulation of On-Chip Power Grid*: Developed efficient solvers for large scale power grid simulation on early design stage, by introducing a fast Poisson solver as an analytical preconditioner for iterative solvers to speedup the simulation [ICCAD'2011, TVLSI'2013]. My work demonstrates about 20X speedups when grid locality is exploited for quasi-Poisson block.
2. *Static Simulation of On-Chip Power Grid*: Developed efficient linear solvers for static analysis of power grid, by introducing an aggregation based algebraic multigrid preconditioned conjugate gradient method to speedup the DC simulation [ICCAD'2011, TAU'2012, TVLSI'2013]. The proposed solver *PowerRush* achieves about tens of speedups than other widely used solvers, and won the first place in the first annual power grid simulation contest on TAU workshop 2011. The contest results show that *PowerRush* not only has a better solving efficiency but also is extremely memory efficient (using only about 40% runtime and 75% memory respectively compared with the second place performance of other simulators).
3. *Transient Simulation of On-Chip Power Grid*: Developed an efficient transient simulator for large scale RLC network [ICCAD'2012], and won the second place in the transient power grid simulation contest on TAU workshop 2012. The contest results show that our proposed simulator is still extremely efficient in memory consumption (with a memory footprint less than half of other teams).

4. *Vectorless Verification of Early Stage Power Grid*: Proposed several efficient vectorless power grid verification techniques for early stage safety check without input current patterns [ICCD'2013, ASPDAC'2013, ASPDAC'2014] (received a Best Paper Award at ICCD'2013), which enables us to verify large scale power grid with uncertainty working mode.

Honors and Awards

Nov. 2013	Ranked as the top 5 teams, in ICCAD Contest 2013, topic: Detailed Placement.
Oct. 2013	National Scholarship, Tsinghua University.
Oct. 2013	**Best Paper Award**, IEEE International Conference on Computer Design, 2013.
Oct. 2012	The IBM Chinese Excellent Student Scholarship.
Jan. 2012	**Second Place**, in Power Grid Transient Simulation Contest on ACM/IEEE TAU Workshop, sponsored by IBM, with award of $600 by IBM, SpringSoft and TSMC.
Oct. 2011	Kwang-Hua Scholarship, First Class, Tsinghua University.
Apr. 2011	**First Place**, in Power Grid Simulation Contest on ACM/IEEE TAU Workshop Sponsored by IBM, with award of $600.
Oct. 2008	National Endeavor Scholarship, Xidian University.
Feb. 2008	Meritorious Winner (First Prize), in Mathematical Contest on Modeling (MCM) by COMAP, U.S.A., Paper Title: When Sudoku Comes across Information Theory.

Professional Activities

Invited reviewer for top journals and conferences in VLSI/CAD:

- ACM/EDAC/IEEE Design Automation Conference (DAC)
- IEEE/ACM International Conference on Computer-Aided Design (ICCAD)
- IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)
- ACM Transactions on Design Automation of Electronic Systems (TODAES)
- IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC)
- IEEE International Symposium on Quality Electronic Design (ISQED)
- Integration, the VLSI Journal

Qualifications and Skills

- Proficient in C/C++, Tcl/TK, Linux Shell, Matlab, Python, Qt, Verilog HDL, HSPICE and LaTeX
- Skilled in EDA Software Development and OpenAccess API
- Skilled in using several Digital System Synthesis and Physical Design Tools
- English Proficiency Test of Tsinghua University II
- College English Test Band 4 (CET-4) & Test Band 6 (CET-6)

Services

July 2013 & Aug. 2012	Student Local Host in Tsinghua for NSF-IRES Program Ceitres @ UC Riverside, Directed by Dr. Sheldon X.-D. Tan
May 2010 - Present	System Administrator for Linux Server of EDA Lab Tsinghua University

Research Project Experiences

1. Power Grid Network Analysis and Verification Techniques for Nanometer SoC Design, National Science Foundation of China. (2013-2016)
2. Development and Application of EDA Platform and System, Important Specific Project in Kernal Electronic Devices, High-end General Application Chips and Foundmental Software Products. (2011-2014)
3. Automatic Routing Techniques for Nanometer Integrated Circuits, National Science Foundation of China. (2010-2012)
4. Efficient Simulation and Optimization Techniques for Large Scale On-Chip Power Grid Network Design, National Science Foundation of China. (2008-2010)
5. Advanced EDA Platform Development, Important Specific Project in Kernal Electronic Devices, High-end General Application Chips and Foundmental Software Products. (2008-2010)

Refereed Journal Articles

1. **Jianlei Yang**, Zuowei Li, Yici Cai, Qiang Zhou. *PowerRush: An Efficient Simulator for Static Power Grid Analysis*, to appear on IEEE Transactions on Very Large Scale Integration (VLSI) Systems. (**TVLSI**, doi:10.1109/TVLSI.2013.2282418)
2. **Jianlei Yang**, Yici Cai, Qiang Zhou, Jin Shi. *Friendly Fast Poisson Solver Preconditioning Technique for Power Grid Analysis.* IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 22, no. 4, pp. 899-912, 2014. (**TVLSI**)
3. **Jianlei Yang**, Yici Cai, Qiang Zhou, Wei Zhao. *A Selected Inversion Approach for Locality Driven Vectorless Power Grid Verification.* Submitted to IEEE Transactions on Very Large Scale Integration (VLSI) Systems. (**TVLSI**)

Refereed Conference Papers

4. **Jianlei Yang**, Liwei Ma, Kang Zhao, Yici Cai, Tin-Fook Ngai. *Early Stage Real-Time SoC Power Estimation Using RTL Instrumentation*, to appear on 20th Asia and South Pacific Design Automation Conference, 2015.
5. Wei Zhao, Yici Cai, **Jianlei Yang**. *Fast Vectorless Power Grid Verification using Maximum Voltage Drop Location Estimation*, Proceedings of 19th Asia and South Pacific Design Automation Conference, pp. 861-866, Singapore, 2014. (**ASP-DAC** 2014).
6. **Jianlei Yang**, Yici Cai, Qiang Zhou, Wei Zhao. *Selected Inversion for Vectorless Power Grid Verification by Exploiting Locality*, Proceedings of IEEE International Conference on Computer Design, pp. 257-263, Asheville, 2013. (**ICCD** 2013, **Best Paper Award**)
7. Wei Zhao, Yici Cai, **Jianlei Yang**. *A multilevel H-matrix-based approximate matrix inversion algorithm for vectorless power grid verification*, Proceedings of 18th Asia and South Pacific Design Automation Conference, pp. 163-168, Yokohama, 2013. (**ASP-DAC** 2013)
8. **Jianlei Yang**, Zuowei Li, Yici Cai, Qiang Zhou. *PowerRush: Efficient transient simulation for power grid analysis*, Proceedings of IEEE/ACM International Conference on Computer-Aided Design, pp. 653-659, San Jose, 2012. (**ICCAD** 2012, **Invited Paper** by Special Session of Power grid simulation and verification for billion-transistor VLSI designs)
9. **Jianlei Yang**, Zuowei Li, Yici Cai, Qiang Zhou. *PowerRush: A linear simulator for power grid*, Proceedings of IEEE/ACM International Conference on Computer-Aided Design, pp. 482-487, San Jose, 2011, (**ICCAD** 2011, **Invited Paper** by Special Session of 2011 TAU Power Grid Contest)

10. **Jianlei Yang**, Yici Cai, Qiang Zhou, Jin Shi. *Fast poisson solver preconditioned method for robust power grid analysis*, Proceedings of IEEE/ACM International Conference on Computer-Aided Design, pp. 531-536, San Jose, 2011. (**ICCAD** 2011)
11. Feifei Niu, Qiang Zhou, Hailong Yao, Yici Cai, **Jianlei Yang**, Chin Ngai Sze. *Obstacle-avoiding and slew-constrained buffered clock tree synthesis for skew optimization*, Proceedings of ACM Great Lakes Symposium on VLSI, pp. 199-204, Lausanne, 2011. (**GLSVLSI** 2011)

Workshop Papers

12. **Jianlei Yang**, Zuowei Li, Yici Cai, Qiang Zhou. *PowerRush: A Linear Simulator for Power Grid*, IEEE/ACM International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems, Taipei, 2012. (**TAU** 2012, **Invited Paper**)

Patents

1. Yici Cai, Qiang Zhou, **Jianlei Yang**, A Transient Simulation Method for On-Chip Power Grid with RCL Network, Apply Number: 201310152859.X, Apply Date: 2013-04-27, Public Number: 103207941A, Public Date: 2013-07-17.
2. Yici Cai, Qiang Zhou, **Jianlei Yang**, Zuowei Li, A Simulation Method for On-Chip Power Grid, Apply Number: 201210073172.2, Apply Date: 2012-03-19, Public Number: 102663166A, Public Date: 2012-09-12.
3. Qiang Zhou, Yici Cai, Zuowei Li, **Jianlei Yang**, A Construction Method of Conductance Matrix for On-Chip Power Grid Simulation, Apply Number: 201210058929.0, Apply Date: 2012-03-07, Public Number: 102646143A, Public Date: 2012-08-22.
4. Qiang Zhou, Yici Cai, Zuowei Li, **Jianlei Yang**, An Adaptive Method of Handling Metal Vias for On-Chip Power Grid Simulation, Apply Number: 201210058540.6, Apply Date: 2012-03-07, Public Number: 102592033A, Public Date: 2012-07-18, Grant Date: 2013-07-24.
5. Yici Cai, Qiang Zhou, **Jianlei Yang**, A Friendly Extraction Method of Specific Parasitic Devices for Analog Integrated Circuits, Apply Number: 201010262309.X, Apply Date: 2010-08-25, Public Number: 1923595A, Public Date: 2010-12-22, Grant Date: 2012-10-24.

Teaching Experiences

- Teaching Assistant, *Numerical Analysis*, Prof. Yici Cai
  Undergraduate Course at Tsinghua University, Spring 2010, Spring 2012, Spring 2014
- Teaching Assistant, *Introduction to VLSI Design*, Prof. Yici Cai
  Undergraduate and Graduate Course at Tsinghua University
  Fall 2009, Fall 2010, Fall 2011, Fall 2012, Fall 2013, Fall 2014
- Teaching Assistant, *The Layout Theories and Algorithms for VLSI*, Prof. Qiang Zhou
  Graduate Course at Tsinghua University, Spring 2011, Spring 2013
- Teaching Assistant, *Design Automation for Digital Systems*, Prof. Qiang Zhou
  Undergraduate Course at Tsinghua University, Spring 2013
- Teaching Assistant, *Program Design and Training*, Prof. Hailong Yao
  Undergraduate Course at Tsinghua University, Summer 2012

References

Available upon request.