Bei Yu

CONTACT INFORMATION

Electronic Design Automation Lab
Department of Computer Science and Technology
Tsinghua University

office: (8610) 62795428
fax: (8610) 62781489
e-mail: disyulei@gmail.com

HOMEPAGE http://tiger.cs.tsinghua.edu.cn/students/yubei/

RESEARCH INTERESTS VLSI Design, Physical Design, Low Power Circuit, Network-on-Chips Design.

EDUCATION

Tsinghua University, Beijing, China

M.S. Department of Computer Science and Technology **Sep. 2007 – present**

- Overall GPA: 89.7/100 (Top 10% of 160+)

University of Electronic Science and Technology of China (UESTC), Chengdu, China

B.S. Major of Information and Compute Science **Sep. 2003 – Jun. 2007**

- Overall GPA: 3.59/4.0, Major GPA: 3.65/4.0(Top 10% of 120+)

PUBLICATIONS

Bei Yu, Sheqin Dong, Song Chen, and Satoshi GOTO, "Voltage and Level-Shifter Assignment Driven Floorplanning", IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, Vol.E92-A, NO.12, Dec. 2009.

Bei Yu, Sheqin Dong, Song Chen, and Satoshi GOTO, "Floorplanning and Topology Generation for Application-Specific Network-on-Chip", to appear in IEEE Proc. Asia and South Pacific Design Automation Conference (ASPDAC), 2010.

Bei Yu, Sheqin Dong, Song Chen, and Satoshi GOTO, "Voltage-Island Driven Floorplanning Considering Level-Shifter Positions", in ACM Proc. Great Lakes Symposium on VLSI (GLSVLSI), pages 51-56, 2009.

Bei Yu, Sheqin Dong and Satoshi GOTO, "Multi-Voltage and Level-Shifter Assignment Driven Floorplanning", in IEEE Proc. International Conference on ASIC(ASICON), 2009.

Tao Lin, Sheqin Dong, Song Chen, **Bei Yu** and Satoshi GOTO, "A Revisit to Voltage Partitioning Problem", *submitted to ACM Proc.Great Lakes Symposium on VLSI(GLSVLSI), 2010.*

HONOURS AND AWARDS

- Guanghua First Class Scholarship, Tsinghua University 2009
- Cadence Second Class Scholarship, Cadence 2009
- Second Prize Excellence Scholarship, Univ. Elec Science & Tech of China 2006
- Second Prize Excellence Scholarship, Univ. Elec Science & Tech of China 2005
- Second Prize Excellence Scholarship, Univ. Elec Science & Tech of China 2004
- Third Prize in ACM Programming Context, Univ. Elec Science & Tech of China 2006
- Third Prize in Mathematical Contest in Modeling, UESTC 2005

ACADEMIC EXPERIENCE

Tsinghua University, Beijing, China

Research Assistant, Advisors: Professor Sheqin Dong **Sep. 2007 – present**

- Design and implementation of floorplanning tool with symmetry constraints, using B*-tree and Sequence Pairs.
- Proposed, implemented and evaluated a two phases placement tool VLSAF to solve voltage and level shifter assignment problem. A convex cost network flow algorithm to assign voltage and a minimum cost flow algorithm to assign level shifter. (relative work was accepted by ACM Proc. GLSVLSI 2009)
- Implemented and evaluated a couple of other approaches to voltage assignment problem.
- Extended VLSAF to a new placement tool MVLSAF by supporting arbitrary number of legal voltages in voltage assignment problems. (relative work was accepted by IEEE Proc. ASICON 2009)
- Co-work with other students, revisited voltage partitioning problem, proposed an optimal algorithm running in polynomial time. (relative work was submitted to ACM Proc. GLSVLSI 2010)

Waseda University, Kitakyushu, Japan

Visiting Student, Graduate School of IPS **Sep. 2008 – Aug. 2009**

- Co-work with other students on Through-Silicon Via Planning for 3-D SoCs (relative work was submitted to IEEE Proc. ISCAS 2010).

- Co-work with other students on developing new communication protocols, which can have significant impact on the overall energy dissipation in Wireless Sensor Networks.
- Proposed, implemented and evaluated a topology generation and floorplanning tool for application-specific Network-on-Chips(NoCs). (relative work was accepted by IEEE Proc. ASPDAC 2010)

JEDA Technologies, Beijing, China

Internship **Jan. 2009 – May.2009**

- Implemented and tested on JEDAcc, which is a code coverage tool for programs written in C or C++ languages.
- Tested on JEDA IDE, which is a pack of integrated GUI tools for JEDAcc.

University of Electronic Science and Technology of China, Chengdu, China

Undergraduate Student **Sep. 2003 – Jul.2007**

- Designed and implemented an online chat room under UNIX environment, which was based on multi-thread.
- Implemented and maintain website of Fujian Jianrong Engineering Consult Company (http://www.jrgczx.com).
- Design and implemented the service system of bank using Java, which had three layers and the communication between each layer was based on the protocol of TCP/IP.

Core Courses

Introduction to Design of VLSI	91/100	Layout Theories and Algorithms for VLSI	88/100
Modern Optimization Algorithm	93/100	Design Automation for Digital System	89/100
Advanced Computer Network	91/100	Advanced Computer Architecture	92/100
Data Structure	97/100	Object Oriented Programming Design	88/100
Software Engineering	91/100	Multimedia Information Technology	93/100
Combinatorics	96/100	Math Experiments and Model Building	98/100
Modern Algebra	94/100	Function of Real Variable	96/100
Numerical Analysis	94/100	Probability Theory and Mathematical Statistics	89/100
Experiment of Database	92/100	Electromagnetic Field and Wave	90/100
Operations Research	93/100	Principle of Automation Control	93/100

Technical Skills

Extensive hardware and software experience in various fields of computer science

Programming: C, C++, Java, UNIX shell scripting, SQL, MATLAB.

Applications: EDA tools (such as Cadence Encounter, Synopsys Design Vision), TEX, LATEX, Microsoft Office, and other common productivity packages for Windows and Linux platforms.