Bringing FPGA Design to Application Domain Experts

FPT 2010 Keynote, Tsinghua University, Beijing

Dr. James Truchard
President, CEO, and Co-founder
National Instruments
Agenda

• NI Vision Overview
• LabVIEW Described
• RIO Architecture Described
• Evolving Design Process and Abstraction
• Application Domain Expert Examples
• The High Speed Streaming Challenge
• Summary
The National Instruments Vision

“To do for test and measurement what the spreadsheet did for financial analysis.”

Virtual Instrumentation

Acquire

Analyze

Present

with NI LabVIEW™
Leveraging Semiconductor Technology

Accuracy (Bits)

Frequency (Hz)

FlexDMM
Precision Audio
Mixed-Signal Suite (Digitizer, Generator, Digital)
RF

Traditional Instruments
NI Products, 2005
NI Products, 2006

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A History of Software Continuity

- **1980**: Instrument Control Interfaces
  - Transistor size decreased by a factor of 2,000

- **1990**: LabWindows™/CVI

- **2000**: NI TestStand
  - RIO

- **2010**: LabVIEW

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The National Instruments Vision Evolved...

Graphical System Design

Virtual Instrumentation
- Instrumentation
- RF
- Digital
- Distributed

Industrial Embedded
- Industrial Control (PAC)
- Machine Control
- Electronic Devices
- Code Generation

Real-time
- Measurements
- Embedded Monitoring
- Hardware-in-the-loop

“To do for test and measurement what the spreadsheet did for financial analysis.”

“To do for embedded what the PC did for the desktop.”

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Engineering Grand Challenges

- Advance health informatics
- Engineer the tools of scientific discovery
- Reverse-engineer the brain
- Provide energy from fusion

- Engineer better medicines
- Provide access to clean water
- Enhance virtual reality
- Restore and improve urban infrastructure

- Develop carbon sequestration methods
- Advance personalized learning
- Make solar energy economical
- Prevent nuclear terror

- Secure cyberspace
- Manage the nitrogen cycle
Graphical System Design
Empowering Users Through Software

LEGO® MINDSTORMS® NXT
“the smartest, coolest toy of the year”

CERN Large Hadron Collider
“the most powerful instrument on earth”

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Platform-Based Design - Berkeley

A. Sangiovanni-Vincentelli, UC Berkeley. Defining Platform Based Design. EEDesign, Feb 2002
High-Level Design Models

Dataflow

C Code

Textual Math

Simulation

Statechart

NATIONAL INSTRUMENTS
LabVIEW™
Graphical System Design Platform

PC/Mac/Linux		PXI		CompactRIO		FlexRIO		Custom

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LabVIEW as a Programming Language

LabVIEW Development Environment

Structured Dataflow
State Diagram
Real-Time
Math Script
Timed Computation
Parallel Processing Multi-Core Ready
Distributed Computation
Front Panel
LabVIEW
LabVIEW Real-Time
LabVIEW FPGA
LabVIEW MPU

Desktop PC
PXI
cRIO, cFP
32-Bit μp
NI Platform for Control

LabVIEW Development Environment

- Control Design & Simulation Module
- System Identification Toolkit
- SoftMotion Module
- Statechart Module
- PID & Fuzzy Logic Toolkit
- Simulation Interface Toolkit
- LabVIEW Real-Time
- LabVIEW FPGA
- LabVIEW MPU

Desktop or SBC
PXI
32-Bit µp

cRIO, cFP

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NI Platform for Signal Processing and Communication

LabVIEW Development Environment
with Connectivity to 3rd-party Math Software

Textual (MathScript)
Signal Processing and Analysis

Graphical (Dataflow)
Signal Processing and Analysis

Signal Processing for Measurements

JTFA, Wavelet,
Time-Series Analysis

Digital Filter Design,
Adaptive Filter Design

Control Design,
Dynamic Simulation

Communications
Modulation, Coding, …

Real-Time Image
Processing / Vision

Sound & Vibration

PC/Mac
Sound Card / Web Cam
NI SPEEDY-33 TI DSK
cRIO, cDAQ
PXI, DC – 6.6GHz
FlexRIO

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Combined Graphical/Textual IP Integration
A Hybrid Approach

- Use Graphical IP
- Integrate Xilinx CORE Gen or Re-use any HDL
- Easily Configure Xilinx CORE Gen IP
- Arbitrary HDL
The Y-Chart System Design Methodology

Application Logic

Analysis & Mapping

Platform Architecture

Performance Evaluation


MoCs for Streaming Applications

Key trade-off: Analyzability vs. Expressibility

High-Performance Computing for Real Time

Supervisory Node

Visualization (User Interface)

Computing Nodes

FPGA

Multicore CPU

FPGA

GPGPU

Multicore CPU

GPGPU

Sensors

Actuators

Sensors

Actuators

Sensors

Actuators

Sensors

Actuators

Sensors

Actuators

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Graphical System Design

Test & Measurement
- Automated Test
- Data Acquisition
- Reconfigurable Instruments

Real-time measurements
- Embedded monitoring
- Hardware in the loop

Industrial Embedded
- Industrial Control (PAC)
- Machine Control
- Medical Devices
- C code generation

Hardware and Software Integration
differentiate our solution

“To do for test and measurement what the spreadsheet did for financial analysis.”

“To do for embedded what the PC did for the desktop.”
The Long Tail for Real-Time Algorithm Development & Deployment

- High Volume, Low Mix
- Large Development Teams
- Highly Customized Hardware

- Low Volume, High Mix
- Small Development Teams
- Custom Design on COTS
- Application Domain Experts

To Do For Embedded

System Flexibility and Price

Number of Systems Deployed

- PXI RIO
- PCI RIO
- CompactRIO
- CompactRIO Integrated
- Single-Board RIO
- ARM targets
- Windows
- Real-time Processor
- FPGA
- I/O
- I/O
- I/O
- Custom I/O

LabVIEW

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High-Speed Data Streaming
• Synchronize memory access
• Fast data links for maximum performance

A/D Technology
• Multirate sampling
• Individual channel triggering

Microprocessors
• Floating-point processing
• Communications
• Multicore technology
• Reprogrammable

FPGAs
• High-speed control
• High-speed processing
• Reconfigurable
• True Parallelism
• High Reliability

I/O
• Custom timing & triggering
• Modular I/O
• Calibration
• Custom modules

 Processor
FPGA
Custom I/O

I/O
I/O
I/O
Leveraging COTS Technologies

- Processor
  - Intel, Freescale, Wind River
  - Multi-core and real-time technology

- Bus
  - PCI/PCIe, Enet, USB, wireless, deterministic Enet
  - Open architecture

- FPGA
  - Xilinx Virtex & Spartan
  - Reconfigurable hardware

- IP
  - Control & signal processing IP & I/O drivers
  - Built-in graphical IP, integrate existing IP

- Custom I/O
  - Analog Devices, Texas Instruments
  - Connect to any sensor & actuator
LabVIEW Real-Time

- Multicore programming
- Analysis, control and communication functions
- Integrate C code and text-based math

LabVIEW FPGA

- Graphical FPGA Design
- Fixed-point processing
- Analysis, control and communication functions
- Integrate VHDL IP

- High-speed data transfer
- Tight timing & synchronization of I/O
Traditional Design Process

Application Domain Experts

Software designers

FPGA designers

ASIC/SoC designers

Packaging designers

Custom IC designers
Evolution of Graphical System Design

Application Domain Experts

- Software designers
- FPGA designers
- Packaging designers
- ASIC/SoC designers
- Custom IC designers
- System designers

Prototyping
Low Volume Design
Operating Systems
Programming Languages
Algorithms/IP
Large Teams
High Risk
Multicore Programming
Idea
Separation of Idea and Implementation
High Integration Cost
Fixed-point algorithms
Fragmented Elements
Untested, Unproven
I/O
Packaging
FPGAs
ASICs
Processors
Custom drivers and middleware
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Moore’s Law Drives IC Abstraction
Increasing Levels of Software Abstraction

- Machine code
- Assembly language
- C
- C++
- C#
- System design platform
System Level Integration of Time

Time Scale

- **Backplane timing**
- **IO synchronized with a global clock**
- **Software programmed FPGAs**
- **Timed loops**
- **Software constructs: FIFOs | Queues**
- **Software structured dataflow**

Flexibility

- Nanoseconds
- Microseconds
- Milliseconds
Parallel Architectures Drive Performance

FPGA Performance (GMACs)

CPU Performance (GFLOPs)

FPGAs

CPUs

2.376 TMACS
Concurrency in LabVIEW

Matrix – Vector Multiply

Compilation

Run Time

Run Queue

Execution Tasks

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How We Map Problems ....
Model of Computation to Idea / Platform

- Pipelined Execution (Signal Analysis)
- Distributed Calculation (Finite Element Analysis)
- Parallel Calculation (Dense Linear Algebra)
Eliminating Artificial Complexity

Text-based Compiler

Source String of Characters

→

Tokens

→

Abstract Syntax Tree

→

Intermediate Code Generator & Semantic Analyzer

→

Optimizer & Code Generator

→

Executable Code

LabVIEW Compiler

Source Dataflow Graph

→

Intermediate Code Generator & Semantic Analyzer

→

Optimizer & Code Generator

→

Intermediate Code & Data Dependency Graph

→

Executable Code

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FPGA-based I/O Applications

- **Clocks**
- **PWM**
- **Counters**
- **Custom Counters**
- **Multiple Scan Rates**
- **Custom Timing and Synchronization**
- **Custom Analog Triggering**
- **Custom Analog I/O**
- **Built-in IP Processing Blocks**
Prototyping Platforms

Reconfigurable I/O, Programmable Hardware
NI CompactRIO
Ideal Platform for Control Design

- Reconfigurable FPGA
- Real-Time Processor
- I/O Modules
High Speed & High Precision Control with LabVIEW Real-Time & FPGA

- Scanning Probe Microscope with PLL
- Ultrastable Atomic Force Microscope
- Nanoimprint Lithography (Tsao)
- Precision Servo-Hydraulic Control
The Challenge  Model Predictive Control (MPC) is an established control technology which requires the solving of a quadratic programming (QP) problem within one sampling period. To solve a QP problem within one sampling period demands a high computational speed for the implementation, especially when MPC is used to control high bandwidth processes. **The Solution**  Through the data flow programming paradigm, LabVIEW can be used to model the MPC algorithm, extract potential parallel execution path and implement the MPC onto FPGA.

Yue Siew Peng, Project Officer
Nanyang, Technological University
Robotics for Manufacturing (MIT)

- Prof. Harry Asada, ME
- LabVIEW Real-Time and LabVIEW FPGA
- CompactRio hardware

Custom motor inside of aircraft wing to help with assembly

Bridge inspection robot walks on the underside of steel surfaces.

Pendulum robot swings over aircraft and tracks the surface profile for inspection
NI Tools Keep Ford at the Forefront of Innovation

- Development of a real-time embedded control system for an automotive fuel cell system
- Verification of the control system with a hardware-in-the-loop (HIL) system
- Compact RIO, PXI, SCXI
- LabVIEW Control Design and Simulation Module, LabVIEW Real-Time, Execution Trace Toolkit

"Ford has a long history with NI, and we have used LabVIEW to develop various aspects of every fuel cell electric vehicle that we produce and to successfully design and implement a real-time embedded control system for an automotive FCS." – Kurt D. Osborne, Ford Motor Company
Controlling the World’s Largest Fuel-Cell Hybrid Locomotive with LabVIEW and CompactRIO

- Control and monitor the safety and operation of a 250 kW fuel-cell locomotive
- CompactRIO, LabVIEW FPGA Module, Real-Time Module
- Complex control algorithms at very fast loop rates

“We chose LabVIEW and CompactRIO because the NI C Series modules with integrated signal conditioning helped us implement fast monitoring of the various I/O points while connecting to a wide range of specialty sensors such as flowmeters and pressure sensors.” Tim Erickson – Vehicle Projects LLC
LabVIEW-based Combustion Engine Control System

- Patrick Borgqvist at Lund University
- VolvoD5 (single cylinder) passenger car size diesel engine
- LabVIEW Real-Time – control of valve timing, heat release calculation for control of combustion timing & engine load, data acquisition & logging
- LabVIEW FPGA – programmable sampling, feedback control of common-rail pressure, and custom counters
- Parallel loops on RT and FPGA
Example Application – Teaching Lab

- UT-Austin, Aerospace Engineering undergrad controls lab
- Prof. Robert Bishop (*co-author of Modern Control Systems* textbook)
- LabVIEW Control Design & Simulation Module, PXI & PCI RIO
Multidisciplinary Teamwork Projects: HOT-V
(Rensselaer Polytechnic Institute)

Theory  Design  Prototype  Deploy

4 Weeks  8 Weeks  1 Week
NI ELVIS Ecosystem

Circuits

BioMed

Control Design

RF/Comm.

Embedded

Green

Digital Electronics

freescale

NI Multisim
A Flexible Prototyping Platform For All Ages

Challenge
42,000 High School Students
6 Week Build

Solution
Graphical System Design with the NI CompactRIO Flexible Prototyping Platform
FPGA-based Real-Time Wind Turbine HIL Simulation

Proof of Concept
Green Engineering
Powered by National Instruments

**MEASURE IT**
- **Acquire** environmental data from thousands of sensors
- **Analyze** power quality and consumption
- **Present** measured data to adhere to regulations

**FIX IT**
- **Design** and model more energy efficient machines
- **Prototype** next-generation energy technologies
- **Deploy** advanced controllers to optimize existing equipment
Tough Real-Time Challenges

Solving the most sophisticated control applications
High-Speed Streaming is Complex Today

• Challenges
  – LabVIEW G model
    • Original specification from algorithm designer
    • Not feasible for highly efficient implementation on FPGA targets

  – Implementation challenges
    • Floating to fixed point conversion
    • Array data to point-by-point data conversion
    • Explicit concurrency representation
    • FPGA target constraints
    • Integration with internal and third-party IP
Domain Expert Expectations for High-Speed Streaming

• High-level DSP representation that matches algorithm theory
  – Algorithms written independently of hardware target
  – Deal in domain terms of token rate, throughput, and latency

• Explore high-level design tradeoffs without diving into implementation details
  – Tune performance with high-level constraints
  – Access the details if needed
The Challenge Going Forward

Application Trends

- 1000’s of parallel tasks
- Large node/channel counts
- High performance requirements
- E.g. streaming DSP applications

Platform Trends

- 100’s of processing elements
- Heterogeneous processors and memories
- Distributed I/O
- E.g. FPGA targets

How to map the tasks and data in a concurrent application to the processing and memory resources on a platform?
Re-use Drives IP Abstraction Levels

Abstraction

Providers

Xilinx
Altera

Almost everyone

Mostly verification IP providers

System solution providers
NI, Xilinx

Hard IPs

PowerPC
DSP ...

RTL/Pin Level IPs

IP-XACT (IEEE 1685)
AMBA, AXI

Domain Specific Abstract IPs
NI actors, Xilinx actors

Transaction Level IPs
SystemC/TLM

PCle, USB, ...

All HDL IPs, ...

AMI, AXI, ...

Domains

Domain Specific Abstract IPs

NI DSP Designer

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Current Challenges of IP Integration

• Fragmented IP that lacks standards
  - Some standards on meta-data and structural interfaces (IP-XACT), and protocols (AXI)
• But vendors not adopting standards to:
  - Describe IP Interface
  - Capability
  - Behavior
  - Provide coherent simulation models
  - Pragmatically provide an integration experience for configuring the IP
  - Interface to high-level description languages
Domain Specific Abstract IP

- Necessity
  - IP reuse is an obvious way to sustain the rapid growth of design complexity
  - IP interoperability and integration are not trivial

- Value
  - A good amount of FPGA (streaming) IPs conforms to dataflow models of computation
    - All the NI IPs (homogeneous SDF)
    - Most of the Xilinx IPs (SDF)
    - Many other DSP-oriented IPs
  - Lots of IPs exist in other MoCs/domains
    - FSM, SR, …
  - Standardizing IPs offers a promising solution

- Viability
  - Promising results from DSP Designer research on Domain Specific Abstract IP integration and possible standards (ADL)
Describe Just Enough IP for the Domain Expert

DSP Designer User

Modeling Concerns:
- MoC Behavior
- Simulation
- Exploration
- Analysis

Describe IP Protocol Details for the Tools

Actor Designer

Implementation Concerns:
- Protocol details
- Cycle accurate behavior
- Optimized Code Gen
Basic Description of IP <IC, OC, II, ET, IE, IP, OP>

<3,2,6,8,T,[1,0,1,0,1,0],[0,1,0,0,0,1]>

token Input Count = 3
Input access Pattern = [1,0,1,0,1,0]

3

in

out

3

2

token Output Count = 2
Output access Pattern = [0,1,0,0,0,1]

Execution Time = 8
Initiation Interval = 6
Is ET Exact = True

ET=8

0 1 2 3 4 5 6 7 8 Time

II=6

IP=[1,0,1,0,1,0]

OP=[0,1,0,0,0,1]
Future Research Challenges

- IP exchange mechanisms that include model and protocol descriptions – standardization needed
- High-level Models of Computations to efficient implementations
- Compilation time
- Fast estimation (performance, area, power, etc.) from high level models
- Multi-level soft-cores and virtual fabrics
- Dynamic partial reconfiguration
- HW/SW operating systems
- Standard floating/fixed point representation and automatic conversion
NI FlexRIO
A Hardware Platform for Streaming Computation

NI FlexRIO Adapter Module
- Interchangeable I/O

NI FlexRIO FPGA Module
- High-speed peer-to-peer data streaming

PXI Platform
- PXIe data streaming rates

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NI FlexRIO Adapter Modules

**Digital**
- 100 MHz DIO
- 200 MHz DIO
- 200 MHz DIO
- Camera Link
- RS-485/422

**Analog**
- 2 ch 100 MS/s AI/AQ
- 32 ch 50 MS/s AI
- 4 ch 250 MS/s AI
- 16 ch 50 MS/s AI
Optical Coherence Tomography Research

Early Cancer Detection with LabVIEW & PXI

K. Ohbayashi
Kitasato University,
Center for Fundamental Sciences

~ 1.5 M FFTs / sec for Real-Time Performance
LTE Base Station Emulator

**Standard PC**
- Multi-Core CPU

**NI PXIe-8108**
- Real-time Dual-Core Controller

**NI PXIe-5641R**
- IF Transceiver

**NI PXI-5610**
- 2.7-GHz RF Up-converter

**NI PXI-5600**
- 2.7-GHz RF Down-converter

**Multi-Core CPU (RT)**
- FPGA

**Higher-Layer Software and Link Control**
- LTE PHY Base Station Tx / Rx

**GUI, System Configuration, Monitoring**

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**On Display at FPT 2010 Demo**
Future | uP and FPGA in one Chip (Xilinx EPP)

Extended Processing Platform

NI RIO Architecture

- I/O
- I/O
- I/O
- Custom I/O
Graphical Dataflow Enables Domain Experts through HLS

The standard combination of IO, high speed buses, processors and FPGAs is an ideal embedded platform.

IEEE 1685 IP-XACT
AMBA AXI4 Interconnect

IP Plug & Play is required to accelerate innovation.
Thank You.
Embedded Landscape

Languages

FPGAs

Drivers

OS

uPs

Buses/Nets

I/O
IP Re-use Across Processing Elements

Languages
- LabVIEW
- Java
- .NET
- Adobe AIR

FPGAs
- XILINX
- ALTERA

Drivers
- OS
- Linux
- Android

uPs
- ARM
- Intel
- PowerPC

Buses/Nets
- AMBA
- PCI Express
- Ethernet
- USB

I/O
- Samsung
- Analog Devices
- Fujitsu